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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,626	05/03/2002	Andy Huang		9685

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EXAMINER	
SHARON, AYAL I	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,626	HUANG, ANDY	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claim 1 of U.S. Application 10/063,626 filed on 05/03/2002 has been presented for examination.
2. An examination of this application reveals that applicant is unfamiliar with patent prosecution procedure. While an inventor may prosecute the application, lack of skill in this field usually acts as a liability in affording the maximum protection for the invention disclosed. Applicant is advised to secure the services of a registered patent attorney or agent to prosecute the application, since the value of a patent is largely dependent upon skilled preparation and prosecution. The Office cannot aid in selecting an attorney or agent.

   A listing of registered patent attorneys and agents is available on the USPTO Internet web site http://www.uspto.gov in the Site Index under "Attorney and Agent Roster." Applicants may also obtain a list of registered patent attorneys and agents located in their area by writing to the Mail Stop OED, Director of the U. S. Patent and Trademark Office, PO Box 1450, Alexandria, VA 22313-1450.

Drawings

3. This application has been filed with informal drawings which are acceptable for examination purposes only. The items in Fig.1 are not legible. Formal drawings will be required if the application is allowed.

Specification

4. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter.

Claim Rejections - 35 USC § 101

5. **Claim 1 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.** An invention which is eligible for patenting under 35 U.S.C. § 101 is in the "useful arts" when it is a machine, manufacture, process or composition of matter, which produces a concrete, tangible, and useful result. The fundamental test for patent eligibility is thus to determine whether the claimed invention produces a "**useful, concrete and tangible result.**" The test for practical application as applied by the examiner involves the determination of the following factors:

    a. "**Useful**" - The Supreme Court in *Diamond v. Diehr* requires that the examiner look at the claimed invention as a whole and compare any asserted utility with the claimed invention to determine whether the

asserted utility is accomplished. Applying utility case law the examiner will note that:

3. the utility need not be expressly recited in the claims, rather it may be inferred.

4. if the utility is not asserted in the written description, then it must be well established.

b. "**Tangible**" - Applying *In re Warmerdam*, 33 F.3d 1354, 31 USPQ2d 1754 (Fed. Cir. 1994), the examiner will determine whether there is simply a mathematical construct claimed, such as a disembodied data structure and method of making it. If so, the claim involves no more than a manipulation of an abstract idea and therefore, is nonstatutory under 35 U.S.C. § 101. In *Warmerdam* the abstract idea of a data structure became capable of producing a useful result when it was fixed in a tangible medium which enabled its functionality to be realized. See MPEP §2106 (A). See also *Schrader*, 22 F.3d at 295, 30 USPQ2d at 1459.

c. "**Concrete**" - Another consideration is whether the invention produces a "concrete" result. Usually, this question arises when a result cannot be assured. An appropriate rejection under 35 U.S.C. § 101 should be accompanied by a lack of enablement rejection, because the invention cannot operate as intended without undue experimentation.

6. The Examiner respectfully submits that under current PTO practice, the claimed invention does not recite *either a tangible or a concrete result.*

a. The claims are not tangible because simply a mathematical construct is claimed.

b. The claims are not concrete because there is no identifiable output. Since there are no results, results are not assured.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claim 1 is rejected as failing to define the invention in the manner required by 35 U.S.C. 112, second paragraph.**

The claim is narrative in form and replete with indefinite and functional or operational language, such as "how to model", "the way to input", etc. The structure which goes to make up the device must be clearly and positively specified. The structure must be organized and correlated in such a manner as to present a complete operative device. The claim must be in one sentence form only. Note the format of the claims in the patents cited.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. The prior art used for these rejections is as follows:

11. Hamoui, A.A. et al. "An Analytical Model for Current, Delay, and Power Analysis of Submicron CMOS Logic Circuits." IEEE Transactions on Circuits and Systems II: Analog and Digital DSP. Oct. 2000. Vol. 47, Issue 10, pp. 999-1007. (Henceforth referred to as "**Hamoui**").

12. "Level 27 SOSFET Model." Star-Hspice Manual – Release 1999.4 Dec. 15, 1999. Printed from http://siloam.han.ac.kr/~young/data/hspice_html/hspice-152.html. (Henceforth referred to as "**SOSFET**").

13. Alinikula, P. et al. "Design of Class E Power Amplifier with Non-linear Parasitic Output Capacitance." IEEE Transactions on Circuits and Systems II: Analog and Digital DSP. Feb. 1999. Vol. 46, Issue 2, pp. 114-119. (Henceforth referred to as "**Alinkula**").

14. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

15. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Hamoui.

16. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by SOSFET.

17. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Alinkula.

18. In regards to Claim 1, Hamoui teaches the following limitations:

> The method of modeling the junction capacitance of the MOSFET and a analysis technique of it for high-speed circuit simulator comprising that
>
> a) the way to input a net-list of the circuit to be simulated

Hamoui teaches (see p.1003, section "VI. Results"):

"The proposed analytical model, implemented in MATLAB, has been tested with a wide range of inverters designed in both a 5-V, 0.8-μm BiCMOS process and a 2.5-V, 0.25-μm CMOS technology."

Examiner interprets that the "way to input [the] netlist" was the MATLAB user interface.

b) creation procedure to make template net-list as the input net-list for external simulator

Hamoui teaches (see p.1003, section "VI. Results"):

"The proposed analytical model, implemented in MATLAB, has been tested with a wide range of inverters designed in both a 5-V, 0.8-μm BiCMOS process and a 2.5-V, 0.25-μm CMOS technology."

Examiner interprets that the "template net-list" was the MATLAB implementation of the inverters.

c) creation procedure to make a lookup table model for the MOSFET

Hamoui teaches (see p.1003, section "VI. Results"):

"The proposed analytical model, implemented in MATLAB, has been tested with a wide range of inverters designed in both a 5-V, 0.8-μm BiCMOS process and a 2.5-V, 0.25-μm CMOS technology."

Examiner interprets that the MATLAB compilation of the inverter netlist corresponds to the claimed "look-up table".

d) how to model the value of the junction capacitance of MOSFET as piecewise constant

Hamoui teaches (see p.1000, section "III. The CMOS Inverter"):

"Consider the CMOS inverter circuit in Fig.2. The effective load C_L includes the drain-bulk junction capacitances of the nMOS and pMOS transistors ... The nonlinear voltage dependent MOSFET parasitic capacitances are replaced by equivalent constant capacitances. Over each MOSFET mode of operation, the intrinsic gate capacitance is assumed to be a constant fraction of the effective gate-oxide capacitance [15]."

Examiner interprets that the "equivalent constant capacitances" that replace the "non-linear voltage-dependent MOSFET parasitic capacitances" corresponds to the claimed "piecewise constant".

19. In regards to Claim 1, SOSFET teaches the following limitations:

The method of modeling the junction capacitance of the MOSFET and a analysis technique of it for high-speed circuit simulator comprising that

a) the way to input a net-list of the circuit to be simulated

SOSFET teaches (see pp.3-6) a netlist

b) creation procedure to make template net-list as the input net-list for external simulator

SOSFET teaches (see p.1-3) the use of the netlist for SPICE

c) creation procedure to make a lookup table model for the MOSFET

Examiner interprets that the SPICE compilation of the inverter netlist corresponds to the claimed "look-up table".

d) how to model the value of the junction capacitance of MOSFET as piecewise constant

SOSFET teaches (see pp.7-8) that "The automatic diode area and resistance calculation estimates the junction capacitance ...The parameters VNDS and NDS allow for a piecewise linear approximation to the reverse junction current characteristics." (see pp.7-8).

20. In regards to Claim 1, Alinkula teaches the following limitations:

The method of modeling the junction capacitance of the MOSFET and a analysis technique of it for high-speed circuit simulator comprising that

a) the way to input a net-list of the circuit to be simulated

Alinkula teaches a netlist (see Fig.5)

b) creation procedure to make template net-list as the input net-list for external simulator

Alinkula teaches the use of the netlist for SPICE (See Section "IV. Analysis Verification, para.1)

c) creation procedure to make a lookup table model for the MOSFET

Examiner interprets that the SPICE compilation of the inverter netlist corresponds to the claimed "look-up table".

d) how to model the value of the junction capacitance of MOSFET as piecewise constant

Alinkula teaches (see Section "V. Conclusions") that "Component values were solved for three grading coefficients (*MJ = 0.5, 0.67, and 0.75*)". Alinikula also teaches that the grading coefficient MJ is used to calculate the value of C_{j0}, the junction capacitance (see Section "III. Class E with Nonlinear Shunt Capacitor", para.2 and Table II).

Conclusion

21. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

22. Ma, S.W. et al. "Piece-Wise Linear Approximation of MOS Nonlinear Junction Capacitance in High-Frequency Junction Capacitance in High-Frequency Class E Amplifier Design." 2003 IEEE Conf. on Electron Device and Solid-State Circuits. Dec. 16-18, 2003. pp.233-236. (The Ma reference post-dates the filing date of the instant application, and therefore does not qualify as prior-art. Section IV of the reference reads upon the claim.)

23. U.S. Patent 6,931,609 to Naruta et al. [The Naruta reference post-dates the filing date of the instant application, and therefore does not qualify as prior-art. Naruta teaches the modeling of a MOSFET (see col.3, lines 18-21), determining the junction capacitance values (see col.3, lines 43-51), and doing so using approximated linear functions (see col.3, lines 55-67).]

24. U.S. Patent 6,928,626 to McGaughty et al. [The McGaughty reference post-dates the filing date of the instant application, and therefore does not qualify as prior-art. McGaughty teaches the modeling of a MOSFET (see col.7, lines 38-41),

determining the junction capacitance values (see col.4, lines 7-26), and doing so using approximated linear functions (see col.4, lines 7-26).]

25. Enz, C. "An MOS Transistor Model for RF IC Design Valid in All Regions of Operation." IEEE Transactions on Microwave Theory and Techniques. Jan. 2002. Vol.50, Issue 1. pp.342-359. (The Enz reference is silent in regards to piecemeal linear analysis of junction capacitance.)

26. Bisdounis, L. "Analytical Transient Response and Propagation Delay Evaluation of the CMOS Inverter for Short-Channel Devices." IEEE Journal of Solid State Circuits. Feb. 1998, Vol.33, Issue 2, pp.302-306. (The Bisdounis reference is silent in regards to piecemeal linear analysis of junction capacitance.)

27. Ismail, M. et al. "Finite GB and MOS Parasitic Capacitance Effects in a Class of MOSFET-C Filters." Proc. of the 33rd Midwest Symposium on Circuits and Systems. Aug.12-14, 1990. Vol.2, pp.938-941. (The Ismael reference is silent in regards to piecemeal linear analysis of junction capacitance.)

28. Boothroyd, A.R. et al. "MISNAN – A Physically Based Continuous MOSFET Model for CAD Applications." IEEE Transactions on CAD of Integrated Circuits and Systems. Dec. 1991. Vol.10, Issue 12. pp.1512-1529. [The Boothroyd reference teaches (see p.1521, section "C. Extrinsic Capacities" and Eq. 62) that the source and drain junction capacities (C_{jS} and C_{jD}) are nonlinear functions.]

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (571) 273- 8300, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

September 2, 2005

Paul L. Rodriguez 9/2/05

Primary Examiner
Art Unit 2125